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Patent, Trademark, Copyright & Related Causes

July 23, 1999

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WASHINGTON, D.C. 20231

Sir:

RE: Docket No. 2418.05-US-01

Transmitted herewith for filing is the patent application of

Inventor (Assignor) : Shinken Okamoto
Title : MEMORY UNIT HAVING MEMORY STATUS INDICATOR

*** This application claims the priority of Japanese Patent No. 10-357944 filed December 16, 1998.

Enclosed are

[X] Certificate of Mailing by Express Mail.
[X] 14 pages of specification with 12 claims and an Abstract.
[X] 3 sheets of [X] formal [ ] informal drawings.
[X] Letter to Commissioner and Form PTO-1449 with cited reference.
[X] Declaration and Power of Attorney.
[X] Small Entity Declaration.
[X] Assignment Recordation Cover Sheet and Executed Assignment.
[X] Our checks in the amounts of $380.00 and $40.00.
[X] Certified Copy of Japanese Pat. Applic. No. 10-357944.
[X] Associate Power of Attorney.
[X] Change of Attorney's Address.
[X] Postcard receipt.

FEE CALCULATION

			Small Entity	Large Entity	Fee Paid
Basic Fee			$380.00	$760.00	$380.00
Total Claims	12-20	0	x 9.00	x 18.00	$ 0.00
Total Independent Claims	2-3	0	x 39.00	x 78.00	$ 0.00
Total Filing Fee					$380.00

DEPOSIT ACCOUNT INFORMATION

The Commissioner is hereby authorized to charge any additional fees for this application to Deposit Account No. 16-0631.

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Patent Docket 2418.05-US-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re. Appln. of : Shinken Okamoto

For : MEMORY UNIT HAVING MEMORY STATUS INDICATOR

Honorable commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

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HAGIWARA SYS-COM CO., LTD.

Date April 20 1999

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Docket No.: 2418.05-US-01

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Invention : MEMORY UNIT HAVING MEMORY STATUS INDICATOR

MEMORY UNIT HAVING MEMORY STATUS INDICATOR

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to a memory unit that is capable of indicating the status of the memory.

Description of the Related Art

Recently, a non-volatile semiconductor memory known as "flash" memory has been developed and has been used in many fields.

The number of times that information, such as data and programs can be written and deleted (the number of write operations) in flash memory is limited and therefore, flash memory has a limited service life with respect to write operations. For example, some flash memories are capable of only 300,000 to 1,000,000 write operations. As the number of actual write operations approaches the upper limit, it becomes impossible to accurately write information (i.e., writing errors will occur), or the stored information may degrade (i.e., memory errors will occur). Therefore, if the useful life of a flash memory is approaching the end of reliable usage, the user will preferably transfer any data stored in the flash memory to a new memory, so that important data is not lost or damaged.

Presently, no proposals have been suggested to accurately notify an operator that the flash memory is approaching the end of its useful life. Instead, calculations of useful life have been based upon estimates of the number of write operations that have been performed in the given environment.

However, if the actual number of write operations is in fact larger than the estimated number, the flash memory may reach the end of its useful life much earlier than the operator anticipated. In this case, the operator may lose important data if the memory is not timely replaced. On the other hand, if the actual number of write operation is instead less than the estimated number, the semiconductor memory may be prematurely replaced.

SUMMARY OF THE INVENTION

It is, accordingly, an object of the invention to provide an improved memory unit.

Preferable, a memory unit is capable of indicating the status of the memory, such as the

number of write operations that have been performed, the data error frequency or the remaining available memory capacity, so that the state of the memory can be reliably determined. Therefore, memory management can be performed efficiently and appropriately.

Preferably, the memory unit comprises a counter or a counting means that is capable of accurately recording the number of write operations that have been performed on the memory. In the alternative, the memory unit may comprise means for determining the number of memory errors or error frequency. The memory unit also may comprise an indicating means for indicating the state of the memory. This indicating means is not limited, and may include for example, an indication light, a display screen or any other appropriate device for communicating to the operator the status of the memory. Preferably, flash memory is utilized with the present teachings, although the present status indicators are useful for all types of memory.

The memory unit also may include means for transferring data to spare memory if the reliability of a particular memory location has been degraded from use.

Other objects, features and advantages of the present invention will be readily understood after reading the following detailed description together with the accompanying drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a view of a representative embodiment of a memory unit according to the present teachings;

FIG. 2 is a perspective view the representative embodiment of the memory unit according to the present teachings;

FIG. 3 depicts a first representative example of a memory status of a flash memory;

FIG. 4 is a first representative flow chart for controlling a display means;

FIG. 5 depicts a second representative example of a memory status of a flash memory; and

FIG. 6 is a second representative flow chart for controlling the display means.

DETAILED DESCRIPTION OF THE INVENTION

Preferably, a memory unit includes memory cells that form a memory and a status indicator or means for indicating the status of the memory. The status indicator can be

utilized to report the status of the remaining useful life of the memory. For example, the memory unit may have a counter that counts the number of write operations that have been performed. The number of write operations then may be communicated to the operator in a variety of ways. For example, the indicating means may simply communicate the number of write operations that have been performed as a number. Alternatively, the indicating means may compare the number of write operations that have been performed to an expected number of write operations that can be performed before the memory cells degrade. The indicating means may indicate to the operator when a certain threshold has been reached. For example, the indicator may warn the operator when 80% or 90% of the upper limit of write operations has been reached.

The memory unit also may include a processing means that provides signals to a display. These signals can represent the useful life of the memory cells. The processing means also may supply signals to the display that represent when remaining capacity in a spare memory area of said memory reaches an upper limit. The signals also could represent an error frequency, such as write errors and memory errors, and the indication means may indicate when the error frequency reaches a predetermined threshold. The processing means can output the signal representing the memory status to an external unit.

Methods for indicating the memory status also are taught. These methods may include (1) counting each write operation, (2) comparing the number of counted write operations to a pre-determined number and (3) indicating the memory status when the number of counted write operations reaches the pre-determined number. Alternatively, methods for indicating a memory status may include (1) monitoring error occurrences for information stored in the memory, (2) determining a frequency of error occurrences, (3) comparing the frequency of error occurrences with a pre-determined frequency and (4) indicating when the frequency of error occurrences reaches the predetermined frequency.

In addition, methods are taught for indicating a memory status in order to shift information stored in the corresponding address to a spare memory area either when (1) the number of write operations for particular addresses reaches a pre-determined number and/or (2) the frequency of error occurrences for information stored in the particular addresses of the memory reaches a pre-determined frequency. Such methods may include (1) determining remaining capacity of a spare memory area whenever information stored in the memory is shifted to the spare memory area, (2) comparing the remaining capacity of the spare memory

area with a pre-determined remaining capacity and (3) indicating when the remaining capacity of the spare memory area reaches the pre-determined remaining capacity.

Each of the additional features and method steps disclosed above and below may be utilized separately or in conjunction with other features and method steps to provide improved memory units and methods for designing and using such memory units. Representative examples of the present invention, which examples utilize many of these additional features and method steps in conjunction, will now be described in detail with reference to the drawings. This detailed description is merely intended to teach a person of skill in the art further details for practicing preferred aspects of the present teachings and is not intended to limit the scope of the invention. Only the claims define the scope of the claimed invention. Therefore, combinations of features and steps disclosed in the following detail description may not be necessary to practice the invention in the broadest sense, and are instead taught merely to particularly describe representative and representative examples of the invention.

A detailed description will now be given of a representative example with reference to the accompanying drawings. FIG. 1 is a view of the representative embodiment showing a memory unit installed in a computer, such as a personal computer. FIG. 2 is a perspective view showing the memory unit in a packaged form.

A memory unit 10 may have flash memories 11-1 through 11-n, a central processing unit (CPU) 12, an indication lamp 14, such as a light emitting diode or other light emitting lamp, and a connection interface 13 for connecting to a computer 20. The computer 20 preferably has a central processing unit (CPU) 21, a first connection interface 22 for connecting to the memory unit 10, a second connection interface 23 for connecting to a display unit 30, such as a CRT, a liquid crystal display or a display lamp, and means for inputting data 40 into the computer, such as a keyboard and a mouse. In this example, the memory connection interface 13 and the computer connection interface 22 may be of the same type as a connection interface by which the computer 20 is connected to the existing memory unit such as a hard disk.

According to the discussion provided above, the flash memories 11-1 through 11-n are representative of a memory or memory cell, the memory processing unit 12 is representative of a processing means, the indication lamp 14 is representative of a status indicator, and the computer 20 and the display unit 30, etc., are representative of an external unit.

In one representative embodiment the memory unit 10 may operate in the following manner. The computer processing unit 21 transmits information to the memory processing unit 12 via the connection interfaces 22 and 13. The data may include, for example, data, programs, write instructions including the write address (logic address), and read instructions including the write address (logic address) to which the information is written. When the memory processing unit 12 receives a write instruction from the computer processing unit 21, the memory processing unit 12 writes the information included in the write instruction to an optional address (physical address) selected from the addresses for the flash memories 11-1 through 11-n. The information is preferably written in flash memories 11-1 through 11-n.

At the same time, the memory processing unit 12 stores the relation of correspondence between the write address (logic address) in which the write instruction is written and an address (physical address) of the flash memories 11-1 through 11-n in which information is written, for example, in an address correlation list (correlation list between logic addresses and physical addresses). Further, when writing information to flash memories 11-1 through 11-n, various methods can be utilized to select an optional address among addresses where information can be rewritten. For example, the lowest-numbered address can always be selected, the addresses can be selected sequentially beginning with the lowest-numbered address (after the highest-numbered address is selected, the lowest-numbered address can be selected again), or the address can be selected at random. In order to efficiently use a flash memory, the addresses are preferably selected so that the same number of write operations have been performed at each address, i.e., data has been written to each memory cell the average number of times.

Further, when the memory processing unit 12 receives a read instruction from the computer processing unit 21, the memory processing unit 12 retrieves the address (physical address) of the flash memories 11-1 through 11-n that corresponds to the write address (logic address) included in the read instruction. The physical address is selected based on the address correlation list and the memory processing unit 12 reads the information written in the retrieved address from the flash memories 11-1 through 11-n. Accordingly, the memory processing unit 12 transmits the read information to the computer processing unit 21 via the connection interfaces 13 and 22. The computer processing unit 21 then operates on the basis of the received information or displays the received information on the display unit 30.

One preferred example of a memory status of the flash memories 11-1 through 11-n is

illustrated in FIG. 3. In FIG. 3, each of the flash memories is divided into a main memory area and a spare memory area. Information to be written in the flash memories 11-1 through 11-n preferably includes a data portion and a redundant portion. The redundant portion preferably contains an error checking code, such as a parity bit. With this error check code, the processor can determine whether any of the data bits is erroneous, and thereby determine whether a writing or memory error has occurred. Further, by using the error check code, erroneous bits can be corrected if the number of erroneous bits is a predetermined number of bits or less.

The memory processing unit 12 usually writes information to an optional address, in which information can be rewritten, in the main memory area of the flash memories 11-1 through 11-n. However, as the number of write operations performed at respective addresses of the flash memories 11-1 through 11-n increases, writing and/or memory errors may occur at such addresses, making it impossible to reliably write and store information. In order to prevent such addresses from being overused, the memory processing unit 12 preferably calculates the number of write operations and/or the error frequency at the respective addresses of the flash memories 11-1 through 11-n. When the number of write operations reaches a set or pre-determined number of times, or when the error frequency reaches a set or pre-determined frequency, no further information is written to the corresponding address. Instead, the memory processing unit 12 can transfer the information stored in the corresponding address to the spare memory area.

When shifting or transferring information to a spare memory address, a correlation between an address (physical address) before shifting and an address (physical address) after the shifting or a correlation between the writing address (logic address) and the address (physical address) after the shifting can be stored, for example, in an address correlation list. A process for shifting the information stored in the respective addresses to the spare memory area and a process for prohibiting writing of information can also be utilized for the spare memory area.

The memory processing unit 12 preferably detects the status of flash memories 11-1 through 11-n and either (1) controls the indication lamp 14 in accordance with the status of the flash memories 11-1 through 11-n or (2) transmits a memory status signal to the computer processing unit 21 of the external computer 20. The computer processing unit 21 can display the status of the flash memories 11-1 through 11-n, for example, on the display unit 30 based

upon the memory status signal generated by the memory processing unit 12.

A representative method for detecting the status of the flash memories 11-1 through 11-n in the memory unit 10 and either (1) controlling the indication lamp 14 in accordance with the detected status or (2) displaying the status of the memory on the display unit 30 also will be described. As noted above, when the number of write operations to the respective addresses of the flash memories 11-1 through 11-n reaches a set or pre-determined number, or when the error frequency at the respective addresses reaches a set or pre-determined frequency, the information written in the corresponding address is shifted or transferred to the spare memory area. As information is stored in the spare memory area, the available capacity of the spare memory area is reduced. When the remaining available spare memory area capacity becomes zero, i.e., the spare memory area is completely filled with information, further information can not be shifted or transferred to the spare memory area. In such case, the operator is preferably notified that the spare memory areas of the flash memories 11-1 through 11-n has no remaining available storage capacity. As a result, the operator is warned to perform maintenance work, such as replacement of the memory unit 10 or the flash memories 11-1 through 11-n, before information is lost or damaged. In addition or in the alternative, the operator can be warned when the number of write operations or the error frequency has reached a set number.

In one preferred embodiment, the indication lamp 14 can be lit in accordance with the results of the comparison between the remaining capacities of the spare memory areas of the flash memories 11-1 through 11-n and the established remaining capacities thereof, so as to display the memory status at the display unit 30. A flow chart shown in FIG. 4 describes one representative example of determining when the indication lamp 14 should be lit, according to this preferred embodiment. Various methods for controlling the indication lamp 14 are available. For example, the indication lamp 14 can simply be turned on or off to represent the status of the memory or a variety of lighting levels or colors can be utilized to provide more detailed status information to the operator. In the flow chart illustrated in FIG. 4, three levels of memory status, i.e. normal status, warning status, and extreme limit status, can be displayed by changing the lighting level or color of the indication lamp 14. Further, if the lighting status of the indication lamp 14 will have more than two levels, either a single or a plurality of indication lamps 14 may be utilized. If a single indication lamp 14 is utilized, the lighting status, for example, colors, periods of blinking, etc., of the indication lamp 14 may

change in accordance with each of the lighting levels. If a plurality of indication lamps 14 are utilized, each indication lamp 14 may correspond to a respective memory status and/or to a respective memory location.

The remaining available capacity of the spare memory areas of the respective flash memories 11-1 through 11-n (Step S1) can be detected while the memory processing unit 12 is operating. For example, the remaining available capacity of the spare memory areas of the respective flash memories 11-1 through 11-n can be detected whenever the memory processing unit 12 shifts information to the spare memory areas of the flash memories 11-1 through 11-n. The detected remaining available capacities can be stored in and read from a memory.

The memory processing unit 12 can determine whether the remaining available capacity of each of the spare memory areas of the respective flash memories 11-1 through 11-n is equal to or greater than a first set remaining available capacity amount (Step S2), which amount may be set to any appropriate pre-determined available capacity amount, such as 20% of the total capacity of the spare memory area. The first set available capacity amount may be selected based on various factors, including the size of the spare memory area. If the remaining available capacity of the spare memory areas of the respective flash memories 11-1 through 11-n is greater than the first set remaining available capacity amount, normal status is preferably displayed (Step S3). For example, a blue indication lamp 14 may be lit.

On the other hand, if any of the spare memory areas of the respective flash memories 11-1 through 11-n has a remaining available capacity that is than the first set remaining available capacity amount, the memory processing unit 12 may then determine whether any one of the remaining capacities of the respective flash memories 11-1 through 11-n is less than a second set remaining available capacity amount (Step S4). For example, the second remaining capacity may be set to 5% of the total capacities of the spare memory area.

If the remaining capacity of each of the flash memories 11-1 through 11-n is equal to or greater than the second set remaining available capacity amount, a warning status may be displayed (Step S5). For example, a yellow indication lamp 14 may be lit to inform the operator that one of the remaining available capacities of the spare memory areas of the respective flash memories 11-1 through 11-n has been reduced and that the memory unit 10 or the flash memories 11-1 through 11-n should be replaced in the near future.

If any one of the remaining available capacities of the respective flash memories 11-1

through 11-n is less than the second set remaining available capacity amount, an extreme limit state may displayed (Step S6). For example, a red indication lamp 14 may be lit to inform the operator that the remaining capacities of the spare memory areas of the flash memories 11-1 through 11-n is approaching zero. Therefore, the operator should immediately replace the memory unit 10 or the flash memories 11-1 through 11-n.

After Steps S3, S5 and S6 are completed, the memory processing unit 12 may determine whether or not a pre-determined diagnosis time has been reached (Step S7). If the diagnosis time is reached, the memory processing unit 12 returns to Step S1 and begins the status check again. The diagnosis time can be set to a variety of values. For example, the diagnosis time may be the time that is necessary to write information in the memory unit 10 or the time necessary to read information stored in the memory unit 10, once each predetermined interval of time has been reached.

The memory status check performed by the algorithm show in FIG. 4 is preferably terminated when the power is interrupted. In addition, steps S2 and S4 may or may not include codes. Further, the set remaining available capacity amount can be set to one or any other appropriate number. If the set remaining capacity is one, the status of the set remaining available capacity can be displayed by switching the indication lamp ON or OFF.

A separate indication lamp 14 can be utilized for each of the respective flash memories 11-1 through 11-n to permit the operator to individually determine the status of each of the spare memory areas of the flash memories 11-1 through 11-n. Therefore, if a single flash memory has reached the limit of its available capacity, that flash memory can be replaced, thereby reducing maintenance costs.

If the number of write operations performed in the flash memories reaches the upper limit of write operations, writing and/or memory errors may occur at an undesirable frequency, thereby making it impossible to reliably store information. Accordingly, the indication lamp 14 also may be lit according to the results of a comparison between the number of write operations to the flash memories 11-1 through 11-3 and the set or pre-determined upper limit. In the alternative, the memory status determined by this comparison may be displayed on the display unit 30.

FIG. 5 shows a register for storing memory status information for the flash memories 11-1 through 11-n according to the total number of write operations performed on the flash memory. Preferably, the memory area of flash memories is divided into the main memory

area and the spare memory area, as in FIG. 3. A register for storing the total number of writing operations is provided in each address of the main memory area and the spare memory area. The memory processing unit 12 writes a new value in a register that corresponds to a respective memory address each time that information is written to or deleted from the respective address. For example, after each write or delete operation, the total number of write operations is incremented by one.

A preferred example for indicating the memory status using the indication lamp 14 is shown in the flow chart of FIG. 6, which provides an algorithm for comparing the total number of write operations and a set or pre-determined upper limit for the respective addresses of the flash memories 11-1 through 11-n. Again, various methods may be employed as a method indicating the memory status using the indication lamp 14 as described above. According to the example provide with respect to FIG. 6, three levels of memory status, i.e., normal status, warning status and extreme limit status, are indicated by changing the lighting state of the indication lamp 14.

The memory processing unit 12 preferably detects the total number of write operations for the respective addresses of the respective flash memories 11-1 through 11-n in Step T1. For example, the number of write operations is read from a number-of-write-operations register that corresponds to a respective address. The memory processing unit 12 determines whether the total number of write operations for each of the respective addresses of the respective flash memories 11-1 through 11-n is less than a first set or pre-determined number (Step T2). The first set number can be set, for example, to 80% of the upper limit of write operations. If each of the respective values is less than the first set number, a normal status is displayed (Step T3). For example, a blue indication lamp 14 may be lit.

If any one of the values is greater than the first set number, the memory processing unit 12 determines whether any one of the respective addresses of the respective flash memories 11-1 through 11-n is greater than a second set or pre-determined number (Step T4). The second set number can be set, for example, to 95% of upper limit of write operations. If any of the values is less than the second set number, a warning status is displayed (Step T5). For example, a yellow indication lamp 14 may be lit to inform the operator that the upper limit of write operations is approaching, and that the memory unit 10 or the flash memories 11-1 through 11-n should be replaced in the near future.

If any one of the values is greater than the second set number, an extreme limit status is

displayed (Step T6). For example, a red indication lamp 14 may be lit to inform the operator that the upper limit of rewrite operations has been reached and that it is necessary to replace the memory unit 10 or the flash memories 11-1 through 11-n.

After Steps T3, T5 and T6 are completed, the memory processing unit 12 may determine whether or not a pre-determined diagnosis time has been reached (Step T7). If the diagnosis time is reached, the memory processing unit 12 returns to Step T1 and begins the status check again. The diagnosis time can be set to a variety of values. For example, the diagnosis time may be the time that is necessary to write information in the memory unit 10 or the time necessary to read information stored in the memory unit 10, once each predetermined interval of time has been reached.

The memory status check performed by the algorithm show in FIG. 6 is preferably terminated when the power is interrupted. In addition, Steps T2 and T4 may or may not include codes. Further, when the value of in an address reaches the set or pre-determined number, the indication lamps 14 are lit or the memory status can be displayed on the display unit 30.

For example, the memory status on the display unit 30 can be displayed to indicate when the total number of write operations for each of the respective addresses in the flash memories 11-1 through 11-n is (1) less than the first set number, (2) greater than the first set number but less than the second set number and (3) more than the second set number. Further, the running total of the number of total write operations for each of the flash memories 11-1 through 11-n can be numerically displayed.

As described above, as the number of write operations increases, the error frequency also increased. If the error frequency reaches the set or pre-determined frequency, the information written in the corresponding address is shifted or transferred to the spare memory area. Thus, the indication lamp 14 can indicate the status of flash memories 11-1 through 11-n in accordance with the results of a comparison between the detected error frequency and the set frequency. In the alternative, the memory status can be displayed on the display unit 30.

A preferred example for indicating the memory status using the indication lamp 14 based upon the detected error frequency for the respective addresses of the flash memories 11-1 through 11-n will be described. Again, various methods may be employed as a method indicating the memory status using the indication lamp 14 as described above. According to this particular example, three levels of memory status, i.e., normal status, warning status and

extreme limit status, are indicated by changing the lighting state of the indication lamp 14.

In response to a read instruction, the memory processing unit 12 can determine whether an error has occurred in either writing the information, or during the storage of the information. Preferably, an error code or parity bit is provided in the read information. If an error has occurred, the memory processing unit 12 can determine the frequency of error occurrences for the address in which the erroneous information was stored, for example, by calculating the total number of error occurrences in the corresponding address during a predetermined period of time.

If the calculated error frequency is less than a first set frequency, a blue indication lamp 14 may be lit, for example, to display normal status. If the calculated error frequency is greater than the first set frequency but less than a second set frequency, a yellow indication lamp 14 may be lit, for example, to display warning status. If the error frequency is greater than the second set frequency, a red indication lamp 14 may be lit, for example, to display extreme limit status. When the calculated error frequency in an address reaches the second set frequency, the memory processing unit 12 can shift the stored information to a corresponding address in the spare memory area. At the same time, the memory processing unit 12 can prohibit any further write operations to that address.

The memory status can also be shown on an external display unit 30. Naturally, by providing this memory status information using an indication lamp 14 or display unit 30, the operator can easily determine the memory status according to the error frequency of flash memories 11-1 through 11-n. In addition, the status of each of the flash memories 11-1 through 11-n can be indicated either using a plurality of indication lamps or by providing individual error frequency reports for each of the flash memories 11-1 through 11-n.

Further, an accumulated value of the number error occurrences in the respective addresses of the respective flash memories 11-1 through 11-n may be used instead of an error frequency value. In this case, the memory status is indicated based upon the results of a comparison between the accumulated value of the number error occurrences and a set or pre-determined number. In this way, the accumulated number of error occurrences in the respective addresses of the main memory areas of the respective flash memories 11-1 through 11-n or all the memory areas may be employed as a frequency of error occurrence.

Moreover, the total number of erroneous bits may be accumulated and used as a frequency of error occurrences. If an error occurs in the information written in the respective

addresses of the flash memories 11-1 through 11-n, the memory processing unit 12 detects the number of erroneous bits contained in the information. If the total number of erroneous bits is less than or equal to a first set or pre-determined number, a blue indication lamp 14 may be lit, for example, to display normal status. If the total number of erroneous bits is equal greater than the first set number, but less than a second set or pre-determined number, a yellow indication lamp 14 may be lit, for example, to display warning status. If the total number of erroneous bits is equal to or greater than the second set number, the extreme limit status is displayed. Herein, for example, the second set number of bits is set to a smaller value by [1] than a predetermined number of bits at which the number of erroneous bits can be corrected to correct data, and the first set number of bits is set to a smaller value by [1] than the first set number of bits. Naturally, the first and second set numbers may be selected according to the designer's preference.

Various representative examples of modifications that can be made to the present teachings without departing from the spirit of the invention will now be described. These representative examples are not intended to be limiting.

The memory status can be indicated using an indication lamp 14 or by displaying on an external display unit 30 or both may be used. While various methods for determining the status of the memory have been described, the designer is free to select other methods for determine the memory status.

Although a plurality of flash memories have been shown in the representative memory units, the number of flash memories may be appropriately established, and may be limited to a single flash memory. In addition, while the described flash memories have been divided into the main memory areas and the spare memory areas, the present teachings are applicable to a flash memory that is not divided into the main memory area and the spare memory area. In this case, information written in an address can be shifted or transferred to a corresponding address when the number of write operations to the respective addresses reaches the set number or when the error frequency at the respective addresses reaches the set frequency. For example, the number of addresses in which the number of write operations has reached the set number of times or the number of addresses in which the error frequency has the set frequency are compared with the first and second set numbers. The memory status indication can then be performed using a similar method in accordance with the results of comparison.

When information was written in an optional address of flash memories 11-1 through

11-n, address management was performed by the memory processing unit 12. However, an external unit also may perform address management, for example, the computer processing unit 21 of the computer 20. In this case, the computer processing unit 21 monitors the number write operations to flash memories 11-1 through 11-n.

As described above, if a memory unit according to the present teachings is used, the memory status can be easily determined and the operator can be informed to timely replace a memory unit or the respective memories. In the alternative, the remaining available capacity of spare memory areas within memories can be easily determined to promptly inform the operator when the memory should be replaced.

What is claimed is:

1. A memory unit having a memory, a memory status indicator and a processor, wherein the processor monitors the status of the memory and communicates memory status information to the memory status indicator.

2. A memory unit as set forth in Claim 1, wherein the memory status indicator is a display, an external display or at least one indicator light.

3. A memory unit as set forth in Claim 2, wherein the processor monitors write operations in the memory and determines when the number of write operations reaches a pre-determined number.

4. A memory unit as set forth in Claim 2, wherein the processor monitors remaining available capacity in the memory and determines when the remaining available capacity is less than a pre-determined amount.

5. A memory unit as set forth in Claim 2, wherein the processor monitors error frequency in the memory and determines when the error frequency reaches a pre-determined number.

6. A method of determining and indicating memory status, comprising the steps of:
calculating a value representative of memory usage;
comparing the calculated number with a pre-determined number; and
changing a memory status indicator when the calculated number reaches the pre-determined number.

7. A method as in claim 6, wherein calculating a value representative of memory usage comprises the step of calculating a total number of write operations performed in a memory.

8. A method as in claim 7 further comprising the step of transferring data stored in a memory location to a spare memory area when the calculated value of the respective address of the memory reaches the pre-determined number.

9. A method as in claim 6, wherein calculating a value representative of memory usage comprises the step of calculating error frequency in a memory.

10. A method as in claim 9 further comprising the step of transferring data stored in a memory location to a spare memory area when the calculated value of the respective address of the memory reaches the pre-determined number.

11. A method as in claim 6, wherein calculating a value representative of memory usage comprises the step of calculating remaining available capacity in a memory.

12. A method as in claim 11 further comprising the step of transferring data stored in a memory location to a spare memory area when the calculated value of the respective address of the memory reaches the pre-determined number.

ABSTRACT OF THE DISCLOSURE

A processing unit 12 that is provided in a memory unit 10 can transfer information that is stored in a corresponding address to a spare memory area and prohibit writing of information into the corresponding address when the number write operations to the respective addresses of flash memories 11-1 through 11-3 reaches a set number or when the error frequency in the information stored in the respective addresses reaches a set frequency. When the remaining capacity of a spare memory area reaches a set capacity, an indication lamp 14 may lit or a memory status signal may be transmitted to a processing unit 21 of a computer 20 and displayed on a display unit 30. The memory processing unit 12 may lit the indication lamp 14 when the number write operations to the respective addresses of flash memories 11-1 through 11-3 reaches a set number or when the error frequency in the information stored in the respective addresses reaches a set frequency.

FIG. 1

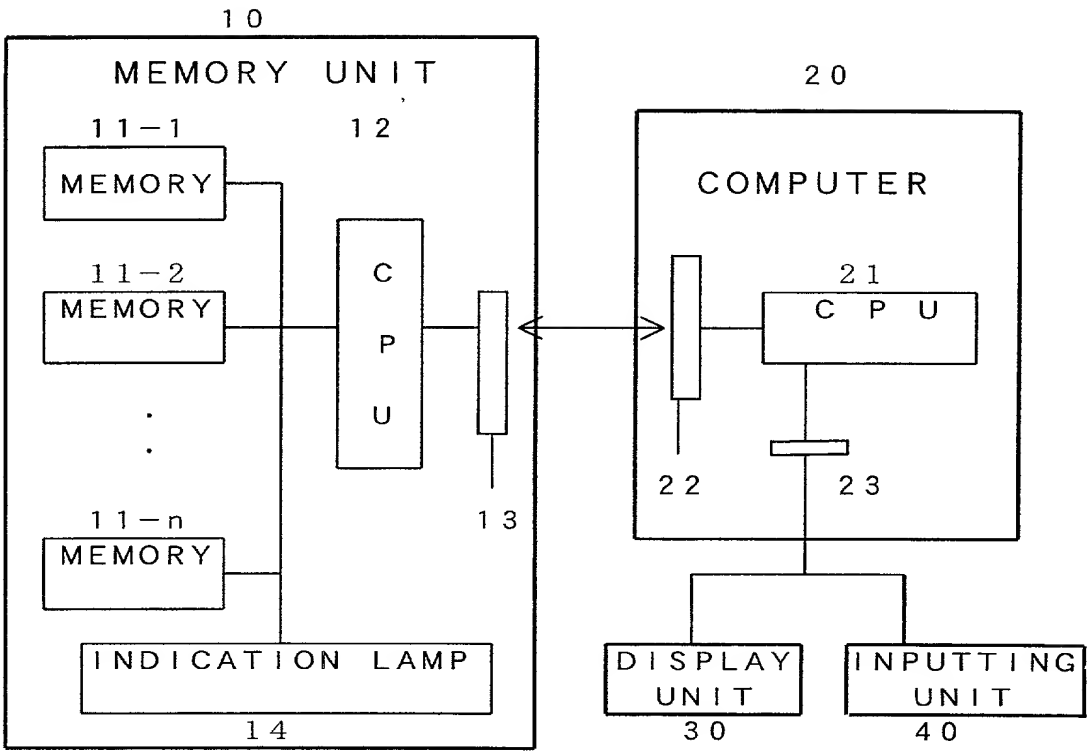

10
MEMORY UNIT
11−1
MEMORY
11−2
MEMORY
11−n
MEMORY
12
CPU
13
INDICATION LAMP
14
20
COMPUTER
21
CPU
22
23
DISPLAY UNIT
30
INPUTTING UNIT
40

FIG. 2

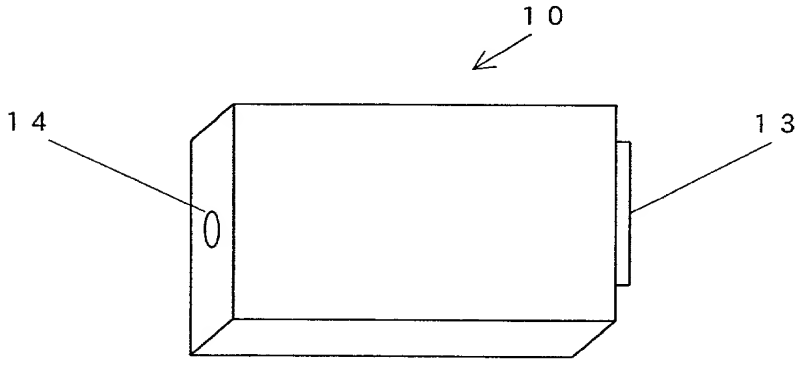

10
14
13

FIG. 3

ADDRESS	INFORMATION
01	
02	
03	
81	
82	

MAIN MEMORY AREAS

SPARE MEMORY AREAS

FIG. 4

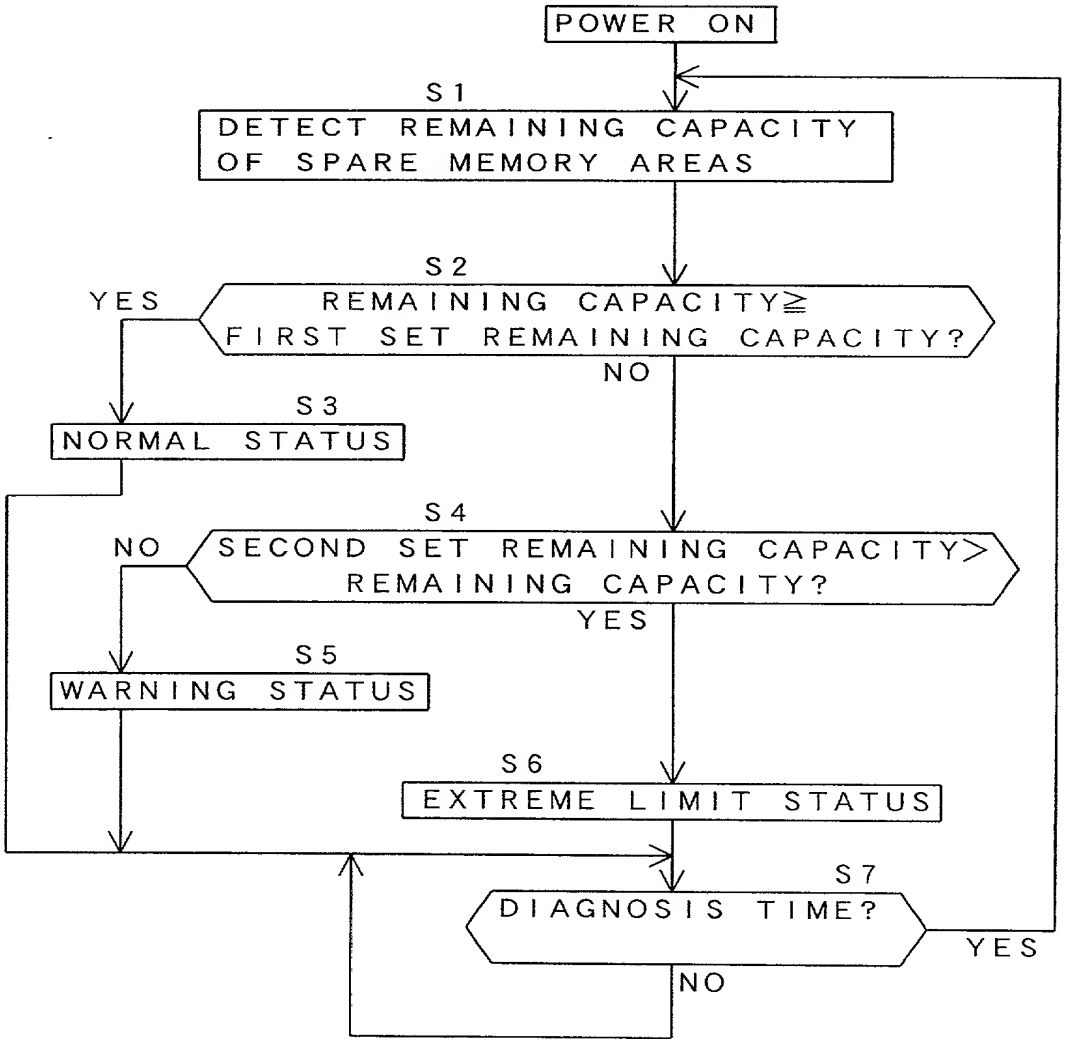
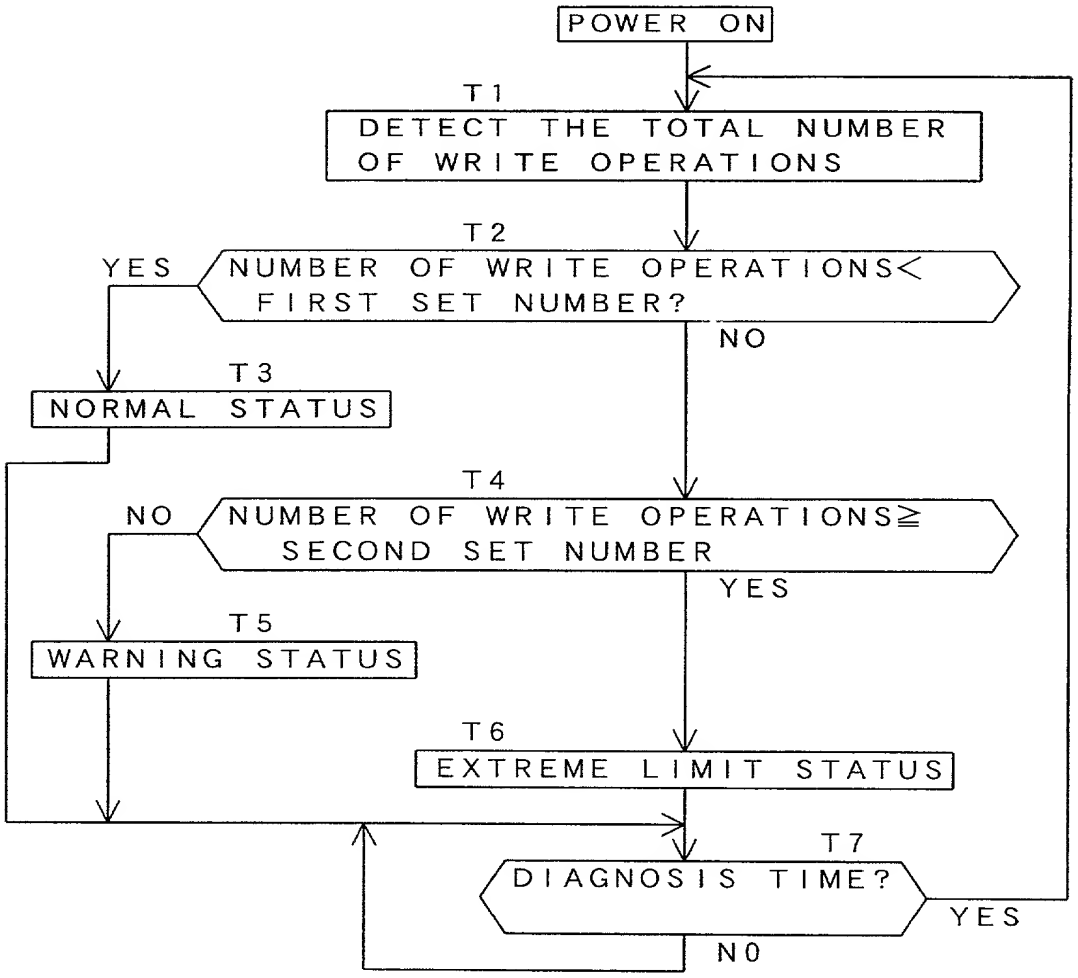


FIG. 5

ADRESS	INFORMATION	TOTAL NUMBER OF RWITE OPERATIONS	
01			MAIN MEMORY AREAS
02			
03			
81			SPARE MEMORY AREAS
82			

FIG. 6



Declaration and Power of Attorney For Patent Application

特許出願宣誓書及び委任状

Japanese Language Declaration

日本語宣誓書

下記の氏名の発明者として、私は以下の通り宣誓します。

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先、国籍は下記の私の氏名の後に記載されたとおりです。

My residence, post office address and citizenship are as stated next to my name.

☐ 下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の氏名が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is Claimed and for which a patent is sought on the invention entitled.

MEMORY UNIT HAVING MEMORY STATUS INDICATOR

上記発明の明細書は、

☐ 本書に添付されています。

☐ __月__日に提出され、米国出願番号または特許協力条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

the specification of which

■ is attached hereto.

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the Contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義される通り、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulation, Section 1.56.

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私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き、下記の米国以外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基く国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application (s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)
Patent Appl. No. 10-357944	Japan	16/12/1998

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Tit application le 35, United States Code, Section 120 of any United States (s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States code Section 112, I acknowledge the duty to disclose Information which is material to Patentability as defined in Title 37, Code of Federal Regulations, Section1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて、本宣誓書中で私が行う表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓をいたします。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may Jeopardize the validity of the application or any patent issued thereon

Japanese Language Declaration
(日本語宣誓書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

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住所	Residence
国籍	Citizenship Japan
郵便の宛先	Post Office Address

(第三以降の共同発明者についても同様に記載し、署名すること)

(Supply similar information and signature for third and subsequent joint inventors)

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Serial No.	:	)
		) OF EVEN DATE
Filed	:	)
For	:	MEMORY UNIT HAVING MEMORY STATUS INDICATOR
Docket No.	:	2418.05-US-01
Additional Fees	:	Charge to Deposit Account No. 16-0631

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

ASSOCIATE POWER OF ATTORNEY PURSUANT TO 37 C.F.R. § 1.34(b)

The undersigned attorney of record in this case hereby grants an Associate Power of Attorney for the purpose of telephone conferences, preparing and filing of papers to assist in the advancement of this application to the following persons:

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Date July 23, 1999

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C7852

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Docket No.	:	2418.05-US-01
Additional Fees	:	Charge to Deposit Account No. 16-0631

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

CHANGE OF ATTORNEY'S ADDRESS

Please change the address and firm name of the attorney of record in this case to:

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C7851